

Tianfang Guo

(281)-608-6947 | taylorguo123@gmail.com | [linkedin.com/in/tfguo439](https://www.linkedin.com/in/tfguo439) | tianfangguo.github.io

EDUCATION

M.S., Computer Engineering, *Texas A&M University*, May 2027

- Computer Engineering and Systems Group.
- Thesis Advisor: Paul Gratz

B.S., Electrical and Computer Engineering, *The University of Texas at Austin*, May 2025

- Computer Architecture and Embedded Systems track.

INTERSHIPS

Design Verification Intern, *Qualcomm*, Summer 2024

- Upgraded a Verilog testbench to a full-featured UVM SystemVerilog testbench for the Hexagon DSP, thereby enhancing scalability and reusability.
- Deepened understanding of real-world processor microarchitecture through hands-on work with cutting-edge designs, gaining valuable insights into hidden complexities and performance optimizations.

Product/Test Engineering Intern, *Texas Instruments*, Summer 2023

- Designed and wrote a code generation script in python that led to time savings of up to two weeks during future new product development cycles.
- Reduced material testing time by analyzing test data and pinpointing potential possible improvements for the existing testing algorithm.
- Gained valuable experience collaborating with a diverse team of engineers in a fast-paced and dynamic environment, fostering effective communication skills and achieving successful project outcomes.

PROJECTS

Hardware Arch for ML: *Sparse GeMM Dataflow Survey*, Spring 2025

- Conducted an in-depth literature review of various sparse GeMM dataflows and accelerator implementations to pinpoint architectural trade-offs.
- Built a Python script for preliminary evaluations of dataflows across varying sparsity levels, directly informing the FPGA implementation roadmap.
- Collaborated with two other students on an IEEE-format final report and jointly delivered the capstone presentation, synthesizing results and hardware design insights.

Senior Design Project: *Computer Architecture Explorer*, Fall 2023 - Spring 2024

- Utilized gem5 and SPEC to benchmark a wide selection of performance metrics by dynamically adjusting various components such as memory/cache hierarchies, pipelines, branch predictors, etc.
- Collaborated with peers to design and create an intuitive interface for students to explore performance data, allowing students to quickly and easily understand how changing parameters impact overall system behavior and performance.

Embedded Systems Design Lab Final project (2nd place): *Laser Tag Game*, Spring 2023

- Collaborated with a team of three other students to design and produce a fully functional and feature-rich multiplayer laser tag game, which interfaced many components such as IR sensors, OLED screen, etc.
- Designed a CAD model using Fusion 360 to serve as an aesthetically pleasing enclosure for the custom PCB and mount the various I/O interfaced to it.
- Voted top two out of over 20 projects at the UT Austin Embedded Systems Design Competition by both peers and professors.

SKILLS

Languages: C/C++, Verilog/SystemVerilog, Python, Java, Assembly (Arm Cortex-M, MIPS), HTML/CSS/JS

Tools: Github, Git, Linux, EAGLE, Fusion 360, Xilinx Vivado, gem5, PyTorch, LLVM, UVM, Atlassian Suite, Agile

Topics: Computer Architecture, uArch, Compilers, OS, Digital Logic, AI/ML, Design Verification

Equipment: FPGAs, Lab Equipment, ATE (*Teradyne J750*), Microcontrollers